WHAT IS CLAIMED IS:

1. Level shifting circuitry, comprising:

a level-shifting section responsive to an input logic signal, such input logic signal having a first voltage level representative of a first logic state or a second voltage level representative of a second logic state, such level-shifting section providing an output logic signal at an output terminal thereof having a third voltage level representative of the first logic state of the input logic signal;

an enable/disable section, responsive to an enable/disable signal, for placing the output terminal at a relatively high output impedance condition independent of the logic state of the input signal during a disable mode.

In one embodiment, the level-shifting section includes an additional transistor. The additional transistor has a control electrode connected to the junction, a first electrode coupled to the source of the third voltage level through the first switching transistor and a second electrode connected to the second electrode of the input transistor. In one embodiment, the input transistor and the additional transistor are of opposite conductivity type.

2. The level shifting circuitry recited in claim 1,wherein the level-shifting section includes:

an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode;

a first switching transistor;

a second switching transistor;

an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and a control electrode coupled to the second electrode of the input transistor, a junction between the output pair of transistors providing the output terminal for the level-shifting circuitry, a control electrode of the second one of the pair of transistors being connected to the first electrode of the input

transistor, the second one of the pair of transistors having a second electrode coupled to the second voltage level through the second switching transistor; and

wherein the first and second switching transistors are fed by the enable/disable signal.

3. The level-shifting circuitry recited in claim 2 wherein the enable/disable circuit includes an inverter, and wherein such inverter is fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor.

4. The level-shifting circuitry recited in claim 3 wherein the inverter is powered by a source of the first voltage level.

5. The level shifting circuitry recited in claim 4 wherein the control electrode of the input transistor is coupled to the source of the first voltage level.

6. The level shifting circuitry recited in claim 4 wherein the inverter comprises:

a level shifter for shifting the level of the enable/disable signal from the first voltage level to the third voltage level and for feeding such third voltage level to the control electrode of the first switching transistor to placing the first switching transistor to a non-conducting condition during the disable mode.